**Lecture 4**

## Components of an MCU

- Program Memory (Flash ROM)

- Non-volatile (Data retained without power)

- ROM – Read Only Memory

- Erasable and rewritable during development

- Data Memory (RAM)

- Usually volatile (not permanent)

- RAM – Random Access Memory

- Very expensive in silicon and power usage

- 1 kB = 1000B

- 1KiB = 1024B

- In/Out Ports

- Address Bus

- CPU

- Clock

## Memory Mapping

- Every register is mapped to a unique 16-bit memory address

- Two architectures

- Von Neumann (Princeton) Architecture

- 1 address bus

- 1 data bus

- Harvard Architecture

- 2 address buses

- 2 data buses

- ROM and RAM each have their own address and data bus

- ARM CPUs use this!

- Comparing the two

- Harvard more efficient

- von Neumann much simpler

- Address bus is 16 bits wide

- Each address expressed as hex numbers from 0x0000 to 0xFFFF

- Total number of registers or 65,536 or 64KiB

- Data bus is also 16 bits wide (16 bit architecture)

- Data bus can transfer a…

- Byte (8 bits)

- Each byte has an address

- Word (16 bits)

- Which part of the word is addressed??

- The byte with the lower address

- Address of a word is always even

- Bytes 0x0000 and 0x0001 form a word of address 0x0000

- Bytes 0xFFFE and 0xFFFF form a word of address 0xFFFE

- Bytes 0x0001 and 0x0002 cannot be accessed as a word

## Endiannes

- About how words are stored in memory

- How is a word (two bytes) ordered over two addresses?

- word 0x1234

- 0x12 more/higher significany byte (MSB or HSB)

- 0x34 lower significant byte (LSB)

- Two ways of storing bytes over two addresses

- Big-Endian Ordering

- HSB at lower address

- LSB at higher address

- Little-Endian Ordering

- LSB at lower address

- HSB at higher address

- MSP430 uses little-endian ordering

- Word 0x1234 is stored as…

- 0x34 at 0x1C00

- 0x12 at 0x1C01

## Memory Mapping (RAM)

- 2048B = 2KiB

- Goes from 0x1C00 to 0x23FF

- Start and end points of RAM

## Memory Mapping (FRAM)

- 48,000B = 48kB

- Starts at 0x4400, ends at 0xFF7F

## Core Registers

- The 16 core registers R0-R15 are 16-bit registers that

- Program Counter (PC/R0)

- Stack Pointer (SP/R1)

- Status Register (SR/CG1/R2)

- Constant Generator (CG2/R3)

- General-Purpose Registers (R4 to R15)

- They have no memory address, are accessed by name